| Notice of Allowability | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/040,582 | GROCHOWSKI ET AL. | |
| | Examiner | Art Unit | |
| | Kandasamy Thangavelu | 2123 | |

***-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--***

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *28 December 2001*.

2. ☒ The allowed claim(s) is/are *1,4-12 and 14-25*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   **Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date September 14, 2001 2004
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☒ Other *Clean copy of allowed claims*.

## DETAILED ACTION

### *Introduction*

1. This communication is in response to the Applicants' communication dated December 28, 2001. Claims 1-25 of the application are pending.

### *Information Disclosure Statement*

2. Acknowledgment is made of the information disclosure statements filed on September 14, 2001 together with a list patents and papers. The patents and papers have been considered.

### *Examiner's Amendment*

3. Authorization for this examiner's amendment was given in a telephone conversation by Mr. Michael Nesheiwat on September 7, 2005.

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to the applicants, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

3. In the specification:

In Page 10, Lines 22-23, "Shifting impulse responses 440, 450, 460 reflects the different times"

has been changed to

-- Shifting impulse responses 440, 450, 460 reflect the different times --

In Page 12, Lines 8-9, "The peak-to-peak current variations in phases 534, 534, 544 are noticeably larger than those associated with loop phases 520, 540, 550"

has been changed to

-- The peak-to-peak current variations in phases 524, 534, 544 are noticeably larger than those associated with loop phases 520, 530, 540 --

4. In the claims:

Replace Claim 1 with:

1. A system to provide power in a specified voltage range to an integrated circuit comprising:

a power delivery network characterized by a response function; and

a device to draw power from the network, the device including:

a first shift register to store values representing a sequence of current amplitudes drawn by the device on successive clock cycles;

an adder having inputs weighted to reflect the response function of the power delivery network, the adder to determine a weighted sum of the sequence of current amplitudes to estimate a voltage provided to the device;

a voltage comparator to compare the estimated voltage to a voltage threshold; and

a throttle unit to adjust operation of the device responsive to the estimated voltage reaching the voltage threshold.

In Claims 2-3:

Delete claims 2 and 3.

In Claim 5, Lines 2-3, "voltage exceeding the upper voltage threshold"

has been changed to

-- voltage exceeding an upper threshold voltage --.

In Claim 6, Lines 2-3, "voltage falling below the lower threshold voltage"

has been changed to

-- voltage falling below a lower threshold voltage --.

Replace Claim 7 with:

7. The system of claim 1, wherein the response function of the power delivery network is represented by n response function amplitudes, and the weighted inputs of the adder comprises n inputs that are weighted proportionally to the n response function amplitudes.

Replace Claim 11 with:

11. The system of claim 10, wherein adder inputs include first and second sets of inputs coupled to outputs of the first and second shift registers, the first set of inputs being weighted proportionally to the current coefficients and the second set of inputs being weighted proportionally to the voltage coefficients.

Replace Claim 12 with:

12. A system to provide power in a specified voltage range to an integrated circuit comprising:

a power delivery network characterized by a response function;

a processor core to execute instructions, the processor core to draw power from the network, responsive to the instructions it executes;

a monitor unit to estimate a voltage provided to the processor core, the monitor unit including:

a current computation unit to track a sequence of current values drawn by the processor core on successive clock cycles; and

a current to voltage computation unit to filter the sequence of current values according to the response function to provide an estimated voltage provided to the processor core;

a threshold comparator to determine if the estimated voltage is within a specified range; and

a throttle unit to adjust operation of the processor core responsive to the estimated voltage not being within the specified range.

In Claim 13:

Delete claim 13.

In Claim 14, Line 1, "The system of claim 13"

has been changed to

-- The system of claim 12--.

In Claim 15, Lines 3-4, "on each of clock cycle of the sequence"

has been changed to

-- on each of the clock cycles of the sequence --.

In Claim 16, Lines 2-3, "on a sequence of m-intervals and an m-entry shift register to store the estimated current amplitudes"

has been changed to

-- on a sequence of m intervals and an m-entry shift register to store the estimated current amplitudes of m intervals --.

Replace Claim 17 with:

17. The system of claim 16, wherein the current to voltage computation unit includes an adder having m inputs, each input being weighted according to the response function of the power delivery network, the adder to estimate the voltage provided to the processor core as a weighted sum of the m current amplitudes provided by the m-entry shift register.

In Claim 18, Line 2, "m-inputs"

has been changed to

-- m inputs --.

In Claim 18, Line 3, "m-intervals"

has been changed to

--m intervals --.

Replace Claim 19 with:

19. The system of claim 17, further comprising a p-entry shift register to store a sequence of p estimated voltages provided by the adder, and to feedback the p estimated voltages to inputs of the adder.

Replace Claim 21 with:

21. An apparatus to estimate a voltage provided to a device in an integrated circuit comprising:

a shift register having n entries to store values representing current amplitudes on n successive intervals;

n weight units, each weight unit to scale a current amplitude value from a corresponding entry of the shift register;

an adder to sum the scaled current amplitudes from the weight units to provide an estimated voltage provided to the device.

Replace Claim 24 with:

24. The apparatus of claim 23, wherein the adder includes p additional inputs and the apparatus further comprises a second shift register having p entries to store a sequence of estimated voltages and to feedback the estimated voltages to the p additional inputs of the adder, the estimated voltages being provided by the adder.

In Claim 25, Line 1, "the additional n and p inputs"

have been changed to

-- the n and p inputs --

**A clean copy of the allowed claims is attached.**

## *Reasons for Allowance*

5. Claims 1, 4-12 and 14-25 of the application are allowed over prior art of record.

6. The following is an Examiner's statement of reasons for the indication of allowable subject matter:

The closest prior art of record shows:

(1) method and apparatus for controlling current demand in an integrated circuit; voltage overshoots and undershoots are caused by changes in power demand when different instruction sequences are executed by IC; the voltage variations are caused during a drastic change of current by the parasitic inductance and is directly proportional to L dI/dt; the method detects if a supply voltage overshoot or an undershoot is present or anticipated and if detected, controlling the current consumed by a circuitry to ensure the power supply voltage remains within acceptable levels; a power consumption control circuitry for controlling current consumed by at least a portion of the power consumption circuitry; the power consumption control circuitry comprises a monitoring circuitry for comparing the power supply voltage to predetermined voltage thresholds; a clock adjusting circuitry coupled to the power consumption control circuitry then adjusts the clock signals provided to the power consumption circuitry; power consumption may be controlled by controlling the global and local clocks, stalling the processor pipeline and interrupting the issue of new instructions (**Blaauw et al.,** U.S. Patent Application 2002/0171407);

(2) a method of analyzing supply voltage drops in a power grid for distributing power to an integrated chip, during the chip design process; providing a library of circuits for use in designing an IC chip and determining a supply current requirement and an operating voltage

range for each circuit in the circuit library; placing a set of circuits from the circuit library in the regions of the power grid; calculating a total node current at each of the ports by summing the current requirements of all of the circuits located in the regions; calculating a node voltage at each of the ports by solving a system of linear equations; imposing a penalty to each voltage having a node voltage outside of a predetermined range; decreasing the voltage and the threshold voltage to lower levels to reduce operating power (**Cohen et al.,** U.S. Patent Application 2002/0112212); and

(3) a method and apparatus for control of rate of change of current consumption of an electronic component; the apparatus includes a processing circuit having an input to receive a throttling signal that throttles the operation of the electronic component; by throttling the activity of the processing circuit during the time of abrupt change in current, the method limits the rate of change of current demand of the component containing the processing circuit; the apparatus also includes a power management circuit which detects a power consumption change of the processing circuit and generates the throttling signal in response to the power consumption change event; the throttle signal controls the pipeline by preventing the instructions from entering the pipeline and by stalling the pipeline; in a processing circuit using clock gating, the clock gating circuitry disables clocks to some portions of the circuits, thus controlling the rate of change of the current (**Horigan et al.,** U.S. Patent 6,304,978).

Additional state of the art reviewed and considered by the Examiner is found in U.S. Patent 6,311,147; U.S. Patent 4,583,111; U.S. Patent 6,536,024; U.S. Patent 6,735,706; U.S. Patent 5,948,106; U.S. Patent 6,636,976; U.S. Patent 6,549,867; U.S. Patent 6,937,971; U.S.

Patent 6,532,439; Sinha et al., "Joule track – A web based tool for software energy profiling", ACM 2001; Steele et al., "Full-chip verification methods for DSM power distribution systems", ACM, 1998.

None of these references taken either alone or in combination with the prior art of record discloses a system to provide power in a specified voltage range to an integrated circuit, specifically including:

"a first shift register to store values representing a sequence of current amplitudes drawn by the device on successive clock cycles;

an adder having inputs weighted to reflect the response function of the power delivery network, the adder to determine a weighted sum of the sequence of current amplitudes to estimate a voltage provided to the device".

None of these references taken either alone or in combination with the prior art of record discloses a system to provide power in a specified voltage range to an integrated circuit, specifically including:

"a current computation unit to track a sequence of current values drawn by the processor core on successive clock cycles; and

a current to voltage computation unit to filter the sequence of current values according to the response function to provide an estimated voltage provided to the processor core".

None of these references taken either alone or in combination with the prior art of record discloses an apparatus to estimate a voltage provided to a device in an integrated circuit, specifically including:

"a shift register having n entries to store values representing current amplitudes on n successive intervals;

n weight units, each weight unit to scale a current amplitude value from a corresponding entry of the shift register;

an adder to sum the scaled current amplitudes from the weight units to provide an estimated voltage provided to the device".

7. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard, can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

Paul L. Rodriguez 9/15/05

Primary Examiner
Art Unit 2125

K. Thangavelu
Art Unit 2123
September 7, 2005